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A Comparison of Lumped-Based Tunable Matching Networks for Dynamically-Load-Modulated Power Amplifiers

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***Abstract*—The power-added-efficiency of power amplifiers deteriorates rapidly as the input power drops. The efficiency at power back-off can be improved by modulating the load dynamically with a tunable matching network. In this work, a novel design method is presented in which the dynamic range of the tunable matching network is plotted on top of the required dynamic load. A comparison between conventional topologies has been performed, and the optimal network is chosen based on its dynamic range and the tunability of its capacitors. As proof of concept, an amplifier has been fabricated and tested achieving a maximum efficiency of 60% and an improvement of 9% with 6 dB of power back-off. The proposed method is useful in designing and optimizing tunable matching networks.**

I. Introduction

As mobile communications are evolving towards the fifth generation (5G), the required data rates are increasing considerably. Such high rates require modulation schemes with high peak-to-average power ratios (PAPR), which is between 7 dB and 10 dB for Long Term Evolution (LTE) signals. Developing RF hardware to transmit such signals with high efficiency is a difficult task.

One of the essential components of the RF transmitter is the power amplifier (PA). The PA consumes most of the DC power in the RF transmitter; therefore, achieving a high efficiency is crucial. The power added efficiency (PAE) of the PA is maximum at the maximum input/output power and deteriorates considerably as the input/output power is reduced. This fact coupled with the high PAPR of the modern digital communications makes the design of efficient PAs very challenging.

There have been many techniques to address this problem over the years. The Doherty technique [1] utilizes an auxiliary transistor, which modifies the load of the main transistor resulting in an optimal loading even at power back-off. An obvious drawback of Doherty, however, is the need for an additional transistor with its bias networks and connections. Another technique is to use a tunable output matching network (OMN) instead of the typically used static network as shown in Fig. 1. If the input power level is sensed, the tunable matching network can *dynamically* transform the static 50 Ω load to the optimal reflection coefficient required by the transistor at each power level. This technique is known as Dynamic Load Modulation (DLM) as is illustrated in Fig. 1 [2].

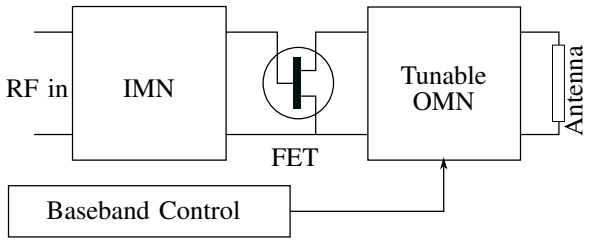

Fig. 1. Schematic of a typical load modulated power amplifier.

It is clear that the design of tunable OMNs is key to the success of the design of DLM PAs. Unlike static matching networks, the optimization of tunable matching networks is not simple. The dynamic range of the tunable matching network needs to be optimized against the optimal reflection coefficients at variable power levels. In this paper, the theoretical tools developed in our previous works are employed to analyze and compare various commonly used matching networks (MNs) [3], [4]. The dynamic ranges of these MNs are compared against the design requirements of a DLM PA to pick the optimal network, which is then realized with high-power GaAs varactors. A GaN-based amplifier has been built and tested as proof of concept, which achieves a maximum PAE of 60% with an improvement of 9% when the input power is reduced by 6 dBs from the maximum value.

II. Output Matching Network Design

A. Source/Load Pull Simulations

The first step in the design of DLM PAs is to determine the optimal input and output terminations for the transistor. Load-pull and source-pull simulations have been performed using the non-linear model of the GaN FET used in this work (CREE CGH40010). The design frequency has been chosen arbitrarily as 0.9 GHz, at which a source-pull has been performed first, while the transistor is biased in class-B conditions. Next, load-pull simulations for the fundamental as well as the second

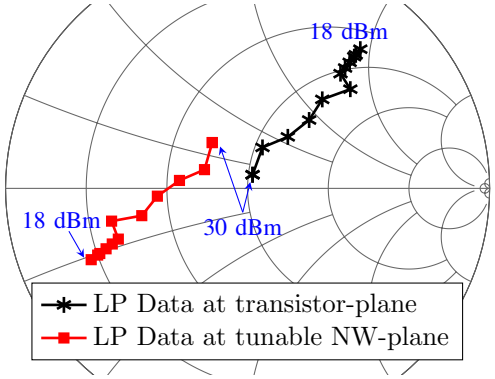

Fig. 2. Load pull simulation data at the transistor-plane as well as the tunable matching network plane (illustrated in Fig. 3).

and third harmonics have been iteratively performed at the maximum input power of 30 dBm. Next, the harmonics have been fixed and load-pull simulations have been carried out at the fundamental frequency for input power levels of (18 -30) dBm. The resultant trace of the optimal reflection coefficients as a function of the input power is plotted in Fig. 2.

B. Static Output Matching Network Design

Since the harmonics are kept constant (with respect to the input power) during the load-pull simulation, a separate static network can be used to terminate them properly. This network consists of two transmission lines and two shunt stubs as shown in Fig. 3. The shunt stubs are designed to provide short circuits at the second and third harmonics and open circuits at the fundamental frequency. The two transmission lines, on the other hand, are designed to provide the required phases for the second and third harmonics. After this network is optimized, the load-pull trajectory provided previously can be transformed beyond this network to the tunable network plane (Fig. 3), which is highlighted in red in Fig. 2. The goal of the dynamic network is to cover this trajectory.

C. Tunable Output Matching Network Design

For the case of the tunable network, a lumped approach is adopted in this work. Since there are many different topologies, which are all commonly used, it is important to select the topology, which provides the optimal performance. Four of these networks are compared in this work and are illustrated in Fig. 4. All of these networks have two tunable capacitors because it is the smallest number that provides a two-dimensional coverage in the Smith chart [3]. The coverage of each network is plotted using the techniques developed in [3], [4] alongside the load-pull trajectory as shown in Fig. 6. The boundaries at which the values of the tunable capacitors are at their minimum or maximum limits are also indicated in the figure. There are many options to realize tunable capacitors such as Micro-electro-mechanical (MEMS), ferroelectric, and varactors. In this work, varactors have been chosen due to their high power handling capabilities. A typical varactor capacitance and quality factor as functions of the

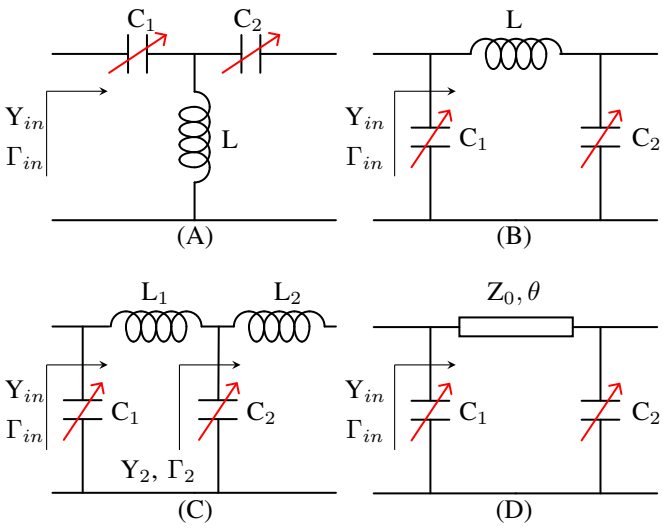

Fig. 4. Schematics of the four topologies considered for the DLM design. (A) T-type. (B) Π-type. (C) Ladder-type. (D) Hybrid Π. $\Gamma_{in} = x + jy$ is the input reflection coefficient and Y_{in} is the input admittance.

reversed bias are plotted in Fig. 5. It can be seen that low capacitances correspond to high bias voltages while high capacitances correspond to low bias voltages. The later, however, is especially sensitive to bias variations because the slope of the capacitance is very high at low bias values. Also, the quality factor of the varactors drops considerable at low bias values as shown in Fig. 5. Therefore, low bias values, which correspond to high capacitance values, should be avoided. Taking this important fact into account, it becomes clear that even though all networks can provide the required coverage, the T-network requires much lower capacitance values and can provide a slightly wider coverage as shown in Fig. 7. Therefore, the T-network has been selected in this stage.

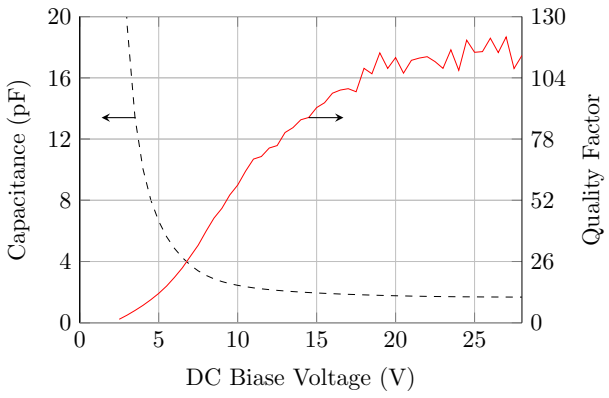

Fig. 5. Measured capacitance and quality factor of a typical silicon varactor (Infineon BB388). This measurement has been performed at 1 GHz.

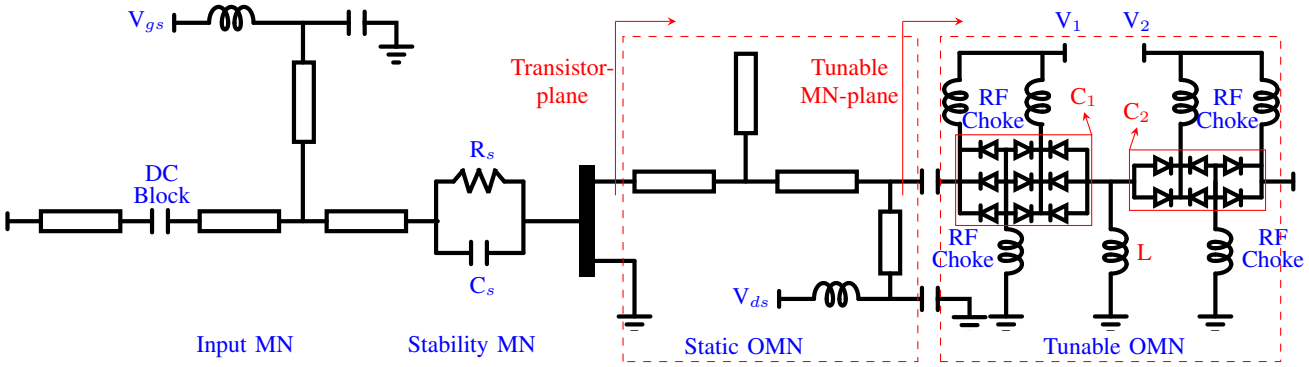

Fig. 3. Schematic of the load-modulated power amplifier with varactors in anti-series configurations to increase their power handling capabilities.

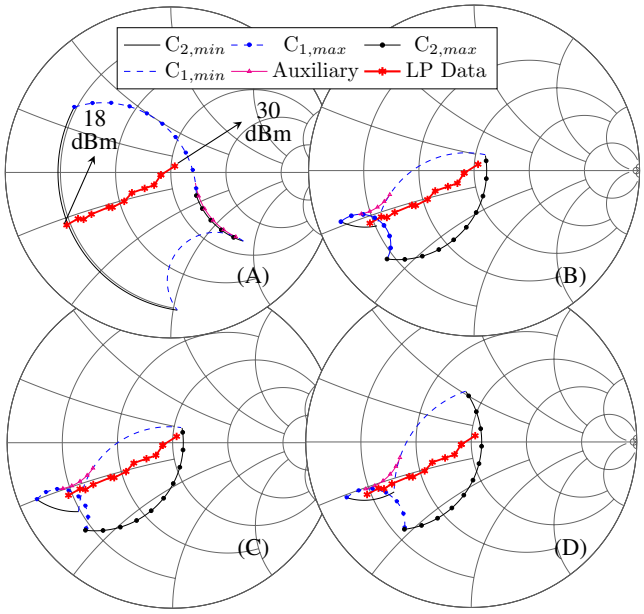

Fig. 6. The coverage of all the networks and the load-pull trajectory (beyond the static NW) of the OMN for input power of 18-30 dBm. (A) T-NW. (B) Π NW. (C) Ladder NW, (D) Hybrid-Π NW.

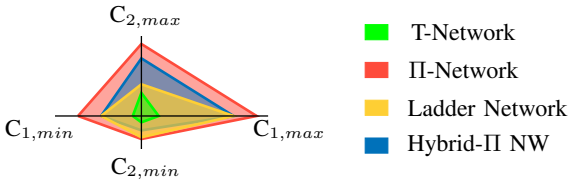

Fig. 7. Comparison of the tuning range of the four networks compared in Fig. 6.

III. Power Amplifier Design and Simulations

A. Tunable Capacitors Realization

From the previous analysis, it has been concluded that the T-network provides the optimal solution in this case. The next step in the design of the PA is to optimize the complete design in a simulation environment. The complete amplifier schematic is illustrated in Fig. 3, where the two parts of the OMN (the static and the tunable network) are highlighted. For the static network, a transmission line-based network has been optimized as illustrated previously. For the tunable network, a T-network topology has been chosen according to the analysis presented in the previous section. Since the amplifier used in this work is intended for high-power applications, varactors with as high breakdown voltages as possible should be selected. In this work, the MTV4090, which has a breakdown voltage of 90 V, has been used. Due to the high peak voltage expected in this design, the capacitors C_1 and C_2 have been implemented in an anti-series configuration to increase their power handling capabilities as shown in Fig. 3 [5]. For C_1, nine varactors have been used in a varactor stack configuration. Since the capacitance requirement on C_2 is slightly lower, only six varactors have been used. Since each varactor can handle up to 90 V of reversed voltage before breaking down, three varactors in an anti-series configuration can handle up to 270 V before either of them breaks down.

B. Power Amplifier Simulation

The complete power amplifier has been simulated in this part using realistic models for the transmission lines, lumped components, and the varactors. In Fig. 8 the power added efficiency (PAE) is plotted as a function of the output power. Two cases have been superimposed: the static matching case, where the amplifier is optimized for the maximum case, and the dynamic case, where the OMN dynamically adapts according to the input power. It can be observed that the amplifier provides almost the same performance for the two cases at the maximum input/output power. When the input/output power is reduced, however, the tunable matching network provides an improved efficiency. When the output power is reduced by 7 dBs from its maximum, the dynamic case offers 18% more efficiency as compared to the static case (Fig. 8). The maximum PAE achieved is about 72 % which drops to about %30 when the input power is reduced from the maximum by 7 dB. At the same conditions, the dynamic matching case results in an efficiency of about 50 %.

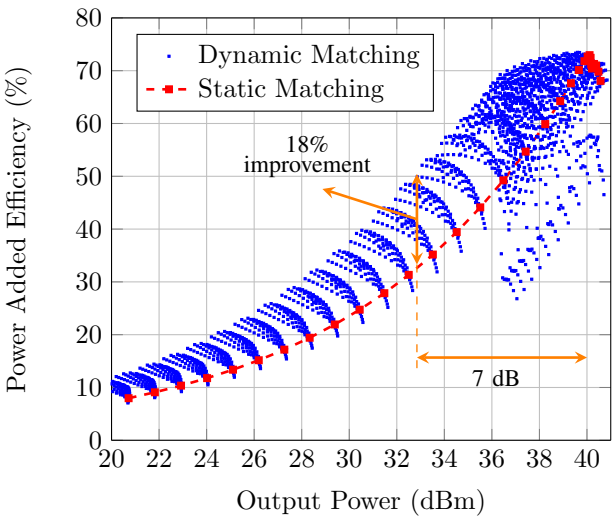

Fig. 8. Simulation results of the load-modulated power amplifier.

IV. Measurements and Discussion

Based on the above-mentioned design, a prototype amplifier has been implemented in a RT/Duroid 5880 substrate with a thickness of 0.79 millimeters as shown in Fig. 9. Two digital power supplies (TTi MX100TP) have been used to provide the bias for the transistor and the varactors. A vector signal generator (Keysight E4438C) have been used to provide a single-tone continuous wave signal, which is amplified using a driver amplifier before fed to the PA being tested. The output of the amplifier is fed to a power sensor. The power supplies, signal generator, and power sensor have all been controlled by a common computer. The bias voltage of each varactor configuration has been swept from 10 Volts to 70 Volts, and the full combination has been measured for variable input power levels. The resultant measurements are plotted in Fig. 10. A maximum efficiency of about 60 % is achieved with an improvement of about 9% when the input power is reduced by about 6 dB. The difference in performance between the simulation and measurement indicates that the model used for the varactors is inadequate. The parasitics incorporated in the model used in this work are frequency and bias independent, which is not an accurate assumption. Therefore, better results would be expected if a more realistic model is used. Also, losses associated with the soldering and integrating such large number of varactors can also contribute to the reduction of the efficiency.

V. Conclusion

In this work, a dynamically load-modulated PA has been designed, built and tested. A novel design approach, in which multiple matching network topologies are compared, has been presented. Based on this design approach, the optimal network topology has been selected and implemented. A maximum measured efficiency of 60 % has been achieved with an improvement of about 9% for a power back-off of 6 dB. The

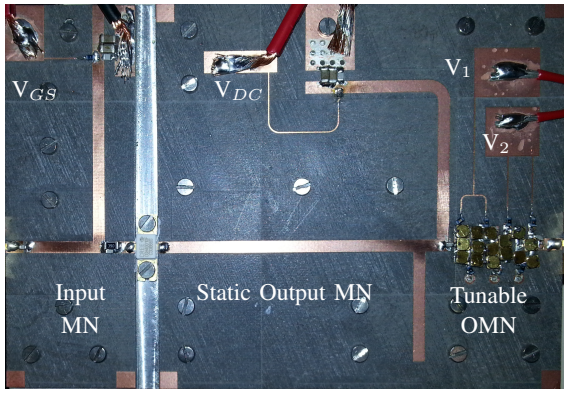

Fig. 9. Photographs of the fabricated amplifier.

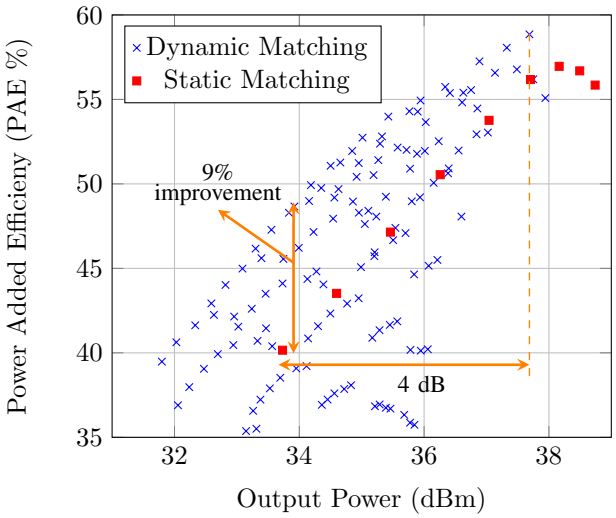

Fig. 10. Measured results of the load-modulated power amplifier.

design approach presented in this work may also be extended to other applications such as tunable antennas.

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